SATA Compliance Test Introduction

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<tr>
<th>Time</th>
<th>Agenda</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:00~2:30</td>
<td>SATA Compliance Test Introduction (Sam Chen)</td>
</tr>
<tr>
<td>2:30~2:45</td>
<td>SATA Certified Logo V1.3 Update (Robert Liu)</td>
</tr>
<tr>
<td>2:45~3:00</td>
<td>SATA UTD V1.4 Information (Robert Liu)</td>
</tr>
<tr>
<td>3:00~3:20</td>
<td>Break</td>
</tr>
<tr>
<td>3:20~3:40</td>
<td>SATA Certified Logo Process (Jina Chen)</td>
</tr>
<tr>
<td>3:40~4:00</td>
<td>SATA SSD Testing (Richard Shen)</td>
</tr>
<tr>
<td>4:00~4:20</td>
<td>Q&amp;A</td>
</tr>
</tbody>
</table>
SATA Compliance Introduction

Sam Chen
Agenda

- Basic Introduction
- Building Block List
- Test Coverage in Compliance
## Basic Introduction

<table>
<thead>
<tr>
<th>Generation</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal Speed</td>
<td>1.5Gb/s</td>
<td>3.0Gb/s</td>
<td>6.0Gb/s</td>
</tr>
<tr>
<td>Compatibility</td>
<td>Gen1 signal</td>
<td>Compatible with Gen1</td>
<td>Compatible with Gen1 and Gen2</td>
</tr>
<tr>
<td>Reference Spec. Version</td>
<td>Serial ATA 2.5</td>
<td>Serial ATA 2.5/2.6</td>
<td>Serial ATA 3.0</td>
</tr>
</tbody>
</table>

- **UTD** – Unified Test Document
  - **Current UTD v1.3**
    - UTD 1.4 is under development
- **MOI** – Method of Implementation
- **ECN** – Engineering Change Notice
Basic Introduction

Device
- hard disk drive, half-height ATAPI device, or slimline ATAPI device
  - Digital/Protocol
  - PHY/Electrical
  - Device Mechanical
  - System Interoperability
- Except 1.8 Inch micro-SATA Drive

Host
- HBA, chipset, add-in controller
  - Digital/Protocol
  - PHY/Electrical
  - Interoperability

Building Block (member only)
- Silicon Solution, IP Silicon Solution
Building Block List

- Building Block
  - Only for Silicon Solution, IP Silicon Solution Vendor
  - Partial Test is acceptable.
  - Also can do the submission
  - The test requirement is the same with complete end products.

- Tested Area:
  - Phy Electrical (PHY/TSG/OOB)
  - Electrical Path (RX/TX)
  - Receiver Jitter Test (RSG)
  - Digital/Protocol (GTR, SSP, ASR, IPM, NCQ)
  - Mechanical (MDI, MDP)
  - System Interoperability
## Building Blocks

<table>
<thead>
<tr>
<th>Interop Program Revision</th>
<th>Company Name</th>
<th>SATA-Io Member</th>
<th>Model Number</th>
<th>Feature Support</th>
<th>Tested Areas</th>
<th>Revision/Firmware Level</th>
<th>Test id</th>
<th>Contact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Date Listed</td>
<td>Product Name</td>
<td></td>
<td>Part Number</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.3</td>
<td>AMD</td>
<td>True</td>
<td>NA</td>
<td>3Gb/s</td>
<td>PHY</td>
<td>NA</td>
<td>email</td>
<td></td>
</tr>
<tr>
<td>1/30/2009</td>
<td>SB800</td>
<td>NA</td>
<td>NA</td>
<td>ASR, IPMd, IPMh</td>
<td>RX/TX, Digital</td>
<td>3060400384</td>
<td>website</td>
<td></td>
</tr>
<tr>
<td>1.3</td>
<td>Intel Corporation</td>
<td>True</td>
<td>NA</td>
<td>3Gb/s</td>
<td>PHY, Sys, Introp</td>
<td>NA</td>
<td>email</td>
<td></td>
</tr>
<tr>
<td>1/30/2009</td>
<td>NA</td>
<td>True</td>
<td>ICH5, ICH6, ICH7, ICH8, ICH9, ICH10</td>
<td>SSC, 3Gb/s</td>
<td>Sys, Introp</td>
<td>306040088</td>
<td>website</td>
<td></td>
</tr>
<tr>
<td>1.3</td>
<td>VIA Technologies Inc.</td>
<td>True</td>
<td>VT8261</td>
<td>3Gb/s</td>
<td>RX/TX, Sys, Introp</td>
<td>NA</td>
<td>email</td>
<td></td>
</tr>
<tr>
<td>1/30/2009</td>
<td>Advanced southbridge with integrated SATA/eSATA ports</td>
<td>True</td>
<td>NA</td>
<td>3Gb/s</td>
<td>RX/TX, Introp</td>
<td>306040094</td>
<td>website</td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td>Silicon Image</td>
<td>True</td>
<td>Sil5744, Sil5723, Sil5734, Sil5733</td>
<td>3Gb/s, IPMd, IPMh</td>
<td>RX/TX, RSG</td>
<td>1.1548</td>
<td>email</td>
<td></td>
</tr>
<tr>
<td>3/25/2008</td>
<td>SteelVine Storage Processor</td>
<td>True</td>
<td>Sil5744, Sil5723, Sil5734, Sil5733</td>
<td>3Gb/s, IPMd, IPMh</td>
<td>RX/TX, RSG</td>
<td>201020113</td>
<td>website</td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td>Synopsys</td>
<td>True</td>
<td>1</td>
<td>NCQ, 3Gb/s, SSP, ASR, IPMd, IPMh</td>
<td>PHY, RX/TX, RSG</td>
<td>1.0i0l</td>
<td>email</td>
<td></td>
</tr>
<tr>
<td>7/30/2008</td>
<td>DWC AHSATA</td>
<td>True</td>
<td>1</td>
<td>3Gb/s</td>
<td>Digital</td>
<td>202040162</td>
<td>website</td>
<td></td>
</tr>
</tbody>
</table>
Test Coverage in Compliance

SATA Compliance Overview

- **PHY/Electrical**: PHY, TX, RX, TSG, OOB and RSG
- **Digital/Protocol**: GTR, NCQ, ASR, SSP and IPM
- **Device Mechanical**: MDI, MDP
- **System Interoperability**
SATA Compliance Overview

PHY/Electrical:
PHY, TX, RX, TSG, OOB and RSG

Digital/Protocol:
GTR, NCQ, ASR, SSP and IPM

Device Mechanical:
MDI, MDP

System Interoperability
Test Concept

- Test Concept
  - Generate specific signal (Test Pattern) for testing

- How to generate test pattern?
  - ULink DriveMaster 2008
    - Quick to issue BIST (FIS Type 58) command
      - BIST T+A+S
      - BIST L
    - Easy to switch between Gen1 and Gen2 mode
  - Generator feature of protocol analyzer
    - Same concept with Driver Master
  - Vendor Specified Method
    - Provide special tool, registry, associate with other device…
### Test Concept (2)

<table>
<thead>
<tr>
<th>Test Concept</th>
<th>HEX before Decode</th>
<th>8B/10B Encode</th>
<th>PHY Layer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HFTP (High Frequency Test Pattern)</strong></td>
<td>4A 4A</td>
<td>D10.2 D10.2</td>
<td>0101010101 0101010101</td>
</tr>
<tr>
<td><strong>MFTP (Mid Frequency Test Pattern)</strong></td>
<td>78 78</td>
<td>D24.3 D24.3</td>
<td>1100110011 0011001100</td>
</tr>
<tr>
<td><strong>LFTP (Low Frequency Test Pattern)</strong></td>
<td>7E 7E</td>
<td>D30.2 D30.2</td>
<td>0111000011 100011100</td>
</tr>
<tr>
<td><strong>LBP ECN18 (Lone Bit Pattern)</strong></td>
<td>0xC8B0C6B</td>
<td>D12.0 D11.4, D12.0 D11.3</td>
<td>0011 0110 1111 0100 0010 0011 0110 1111 0100 0011</td>
</tr>
</tbody>
</table>
PHY / TSG

PHY – Phy General Requirements
- Unit Interval
- Frequency Long Term Stability
- Spread-Spectrum Modulation Frequency
- Spread-Spectrum Modulation Deviation

TSG – Transmit Signal Requirements
- Differential Output Voltage
- Rise/Fall Time
- Differential Skew
- AC Common Mode Voltage (Gen 2 product only)
- Rise/Fall Imbalance (Gen 2 product only)
- Amplitude Imbalance (Gen 2 product only)
- Total Jitter / Deterministic Jitter
OOB (1)

- OOB – Out-of-Band Signaling
  - COMRESET/COMINIT
  - COMWAKE
OOB (2)

COMRESET/COMINIT

T1 : 160UI=106.7ns nominal

T2 : 480UI=320ns nominal

COMWAKE

T1 : 160UI=106.7ns nominal

T1 : 160UI=106.7ns nominal
RSG – Receiver Signal Requirements

• Receiver Jitter Test

• No more than zero frame errors for all four frequencies below.
  5MHz
  10MHz
  33MHz
  62MHz
TX / RX – Transmit / Receiver Requirements

- Pair Differential Impedance (Gen 1 product only)
- Single-Ended Impedance (Informative)
- Differential Mode Return Loss
- Common Mode Return Loss (Gen 2 product only)
- Impedance Balance (Gen 2 product only)
SATA Compliance Overview

PHY/Electrical:
PHY, TX, RX, TSG, OOB and RSG

Digital/Protocol:
GTR, NCQ, ASR, SSP and IPM

Device Mechanical:
MDI, MDP

System Interoperability
GTR - General Test Requirements

- All Serial ATA devices shall meet the test requirement within this section to confirm Serial ATA interoperability.
  - Software Reset
  - 3GB/s Backwards Compatibility
  - DMA Protocol Support
  - General SATA Support
  - Unrecognized FIS receipt
NCQ - Native Command Queuing

- The Native Command Queuing (NCQ) test requirements are determined by the requirements of the feature as defined in Serial ATA Revision 2.6.
- Only for Hard Disk Drive
ASR - Asynchronous Signal Recovery

- COMINIT response interval
- COMINIT OOB interval

<table>
<thead>
<tr>
<th>Time</th>
<th>Frame 973261</th>
<th>01.554 300 350</th>
<th>A</th>
<th>Start</th>
<th>Start</th>
<th>Split</th>
<th>END</th>
<th>COMINIT/COMRESET</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>17.966 µs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Time</th>
<th>Frame 973262</th>
<th>01.554 318 317</th>
<th>A</th>
<th>Start</th>
<th>Start</th>
<th>COMINIT/COMRESET</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.715 µs</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Time</th>
<th>Frame 973263</th>
<th>01.554 321 032</th>
<th>A</th>
<th>Start</th>
<th>Start</th>
<th>COMWAKE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.330 µs</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Time</th>
<th>Frame 973264</th>
<th>01.554 322 352</th>
<th>A</th>
<th>Start</th>
<th>Start</th>
<th>ELECTRIC IDLE OFF</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>552,500 ns</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Time</th>
<th>Frame 973265</th>
<th>01.554 322 905</th>
<th>A</th>
<th>Start</th>
<th>Start</th>
<th>COMWAKE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.357 µs</td>
</tr>
</tbody>
</table>
SSP - Software Settings Preservation

- For device support this optional feature, the software settings that shall be preserved across COMRESET, to avoid software settings lost without knowledge in the case of a synchronous loss of signal.

<table>
<thead>
<tr>
<th>Test Item</th>
<th>HDD</th>
<th>ODD</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSP-01: Initialize Device Parameters</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>SSP-02: Read/Write Stream Error Log</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>SSP-03: Security Mode State</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SSP-04: Set Address Max</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>SSP-05: Set Features-Write Cache Enable/Disable</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SSP-06: Set Features-Set Transfer Mode</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SSP-07: Set Features-Advanced Power Management Enable/Disable</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SSP-08: Set Features-Read Look-Ahead</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SSP-09: Set Features-Release Interrupt</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SSP-10: Set Features-Service Interrupt</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SSP-11: Set Multiple Mode</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>
IPM - Interface Power Management

- HIPM - Host Initiated Interface Power management
- DIPM - Device Initiated Interface Power management
  - Partial
  - Slumber
SATA Compliance Overview

PHY/Electrical:
PHY, TX, RX, TSG, OOB and RSG

Digital/Protocol:
GTR, NCQ, ASR, SSP and IPM

Device Mechanical:
MDI, MDP

System Interoperability
Mechanical

📍 Test Area

- Location
- Dimension
SATA Compliance Overview

- **PHY/Electrical**: PHY, TX, RX, TSG, OOB and RSG
- **Digital/Protocol**: GTR, NCQ, ASR, SSP and IPM
- **Device Mechanical**: MDI, MDP
- **System Interoperability**
The purpose of the System Interoperability test is to ensure a product actually operate.

- The Interoperability test will be performed under DOS mode.
- Long Framed COMP Pattern
  - 8KB, 64KB, 256KB, 1MB, 16MB
- MD5 checksum

```
12/23/2006 Interop CD Test $Revision: 1.5 $ on device
Starting time = 00:24:53
MD5 check file*.img PASSED
MD5 check file*.img PASSED
Ending time = 00:36:10
All tests pass
Total execution time = 677
Total number of loops = 2
Total MB of data transfer = 177.373184
```
Reference documents


Interoperability Documentation v1.3

- SATA Interoperability Program Revision 1.3 - Policy Document v1.0
- SATA Interoperability Program Revision 1.3 - Unified Test Document v1.0

Additional text procedures and tool information is available for SATA-IO Member Download from the Logo WG Web page. Please log onto the Members Only area for access to these tests and documents.

<table>
<thead>
<tr>
<th>Vendor, Model</th>
<th>Ver</th>
<th>Date</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Agilent DSA92044</td>
<td>1.0</td>
<td>6/28/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Tektronix</td>
<td>1.0</td>
<td>5/25/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>LeCroy</td>
<td>1.0</td>
<td>6/05/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Agilent 861000</td>
<td>1.0</td>
<td>10/23/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Tektronix CSA8200</td>
<td>1.0</td>
<td>5/29/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Synthesys 7500B</td>
<td>1.0</td>
<td>12/18/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Tektronix AWG7122B</td>
<td>1.0</td>
<td>5/22/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Agilent NH903 J-BERT</td>
<td>1.0</td>
<td>5/29/2008</td>
<td>Approved</td>
</tr>
</tbody>
</table>

Device Digital I.3 - GDR/NCQ/ASR/SSID/PIM - (updated_IPM)
<table>
<thead>
<tr>
<th>Vendor, Model</th>
<th>Ver</th>
<th>Date</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Elnk</td>
<td>1.0.1</td>
<td>5/27/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>LeCroy</td>
<td>1.0</td>
<td>2/19/2009</td>
<td>Approved</td>
</tr>
</tbody>
</table>

Host Digital I.3 - ASR/PIM
<table>
<thead>
<tr>
<th>Vendor, Model</th>
<th>Ver</th>
<th>Date</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Elnk</td>
<td>1.0.1</td>
<td>9/10/2008</td>
<td>Approved</td>
</tr>
</tbody>
</table>

System Interop I.3 - same as 1.1
Device Mechanical I.3 - MDP/MDP - S3kline
Cable Electrical - 1.0 - Same as 1.0
Cable Mechanical Inspection 1.3 - MCI-91
Cable Mechanical Insertion 1.3 MCI-22/03/04
Cable Mechanical Pull-out 1.3 - MCI-03
Supporting 1.3 - new board pattern
Thank you

Coming Up:

• SATA Certified Logo V1.3 Update
• SATA UTD V1.4 Information

Robert Liu
SATA Certified Logo V1.3 Update

Robert Liu
• Submission Type
• SPEC & MOI update
• Electronic Tests update
• Digital Test update
• Test Failure Statistics
• Test Solution
• Product Class
  
  - Device
    • 2.5” HDD or SSD
    • 3.5” HDD
    • Half-height ATAPI device
    • Slimline ATAPI device
  
  - Host
    • Desktop
    • Motherboard
Submission Type

- Building Block Listing
  - Target
    - Silicon or IP Vendor
  - Product Type
    - Bridge
    - Port Multiplier
UTD 1.3 Update

• SPEC & MOI
  – Change Reference SPEC from SATA 2.5 to 2.6
  – UTD 1.3
    • Add OOB-01 Level Calibration as **normative**
    • Add 5MHz into RSG test as **normative**
    • Add Host Digital as **normative**
    • Add uSATA as **informative** but may become **normative**
    • Add eSATA as **informative**
Electronic Tests

• PHY General Requirements

  – PHY-02: Frequency Long Term Stability
    • V1.2: For both SSC and Non-SSC product
    • V1.3: Only for Non-SSC product

  – PHY-04: Spread-Spectrum Modulation
    • V1.2: 0ppm to -5000ppm
    • V1.3: 350ppm to -5350ppm
Electronic Tests

• PHY Transmit Signal Requirements
  – TSG-07: TJ at Connector, Clock to Data, fbaud/10
    • V1.2: Informative
    • V1.3: No longer required
  – TSG-08: DJ at Connector, Clock to Data, fbaud/10
    • V1.2: Informative
    • V1.3: No longer required
  – TSG-09/11: TJ at Connector, Clock to Data
    • V1.2: Fbaud/500
    • V1.3: Apply Jitter Transfer Function setting
  – TSG-10/12: DJ at Connector, Clock to Data
    • V1.2: Fbaud/500
    • V1.3: Apply Jitter Transfer Function setting
• Jitter Transfer Function Calibration

  – Introduction
    • Standard jitter transfer function requirement
    • Get better correlation between different jitter measurement systems

  – Effect
    • ECN-008
    • Must be done once prior to measure TSG-09 ~ TSG-12
Electronic Tests

• PHY OOB Requirements
  – OOB-01: Level Calibration
    • V1.2: Not required
    • V1.3: Required before doing the testing
  – OOB-03: COMINIT/RESET and COMWAKE Transmit Burst Length
    • ECN17: OOB Burst/Gap Duration Clarification
Electronic Tests

- OOB Burst/Gap Duration Clarification
  - SATA Rev 2.6 ECN017

Figure 1: Captured OOB burst showing +100mV and -100mV burst width asymmetry. (Bits in blue are not included in width if +100mV threshold is used.)
**Electronic Tests**

- **PHY Transmitter/Receiver Requirements**
  - **TX/RX-02: Single Ended Impedance**
    - V1.2: Informative
    - V1.3: Obsolete
  - **Differential Mode Return Loss**
    - V1.2: No define for eSATA
    - V1.3: Informative for eSATA
  - **Common Mode Return Loss**
    - V1.2: No define for eSATA
    - V1.3: Informative for eSATA
  - **Impedance Balance**
    - V1.2: No define for eSATA
    - V1.3: Informative for eSATA
**Electronic Tests**

- PHY Receive Signal Requirements
  - Amplitude Calibration
    - V1.2: No define for eSATA.
    - V1.3: Informative (240mV) for eSATA
  - Sine jitter source frequencies
    - V1.2: 10MHz, 33MHz, 62MHz
    - V1.3: 5MHz, 10MHz, 33MHz, 62MHz
  - Framed COMP pattern
    - V1.2: 4 ALIGN (Old LBP)
    - V1.3: 2ALIGN (SATA Rev 2.5 ECN18 LBP)
      - 4 ALIGN need waiver request
• Digital

  – Test Software Version
    • V1.2: DriveMaster 2006
    • V1.3: DriveMaster 2008

  – Device Test Script
    • V1.2: Digital Test Script v1.6 for UTD1.2
    • V1.3: Digital Test Script v1.7 for UTD1.3

  – Host Test Script
    • V1.2: Not a requirement
    • V1.3: Digital Host V1.3
# Test Failure Statistics (Physical)

<table>
<thead>
<tr>
<th>Test</th>
<th>IW#5 PASS</th>
<th>IW#5 FAIL</th>
<th>IW#6 PASS</th>
<th>IW#6 FAIL</th>
<th>Total PASS</th>
<th>Total FAIL</th>
<th>% Pass</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHY-01a : Unit Interval - Gen 1</td>
<td>59</td>
<td>0</td>
<td>47</td>
<td>0</td>
<td>106</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>PHY-01b : Unit Interval - Gen 2</td>
<td>50</td>
<td>0</td>
<td>39</td>
<td>0</td>
<td>89</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>PHY-02 : Frequency Long Term Stability</td>
<td>47</td>
<td>0</td>
<td>38</td>
<td>0</td>
<td>85</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>PHY-03 : Spread-Spectrum Modulation Frequency</td>
<td>15</td>
<td>0</td>
<td>9</td>
<td>1</td>
<td>24</td>
<td>1</td>
<td>96%</td>
</tr>
<tr>
<td>PHY-04a : Spread-Spectrum Modulation Max Deviation</td>
<td>15</td>
<td>0</td>
<td>10</td>
<td>0</td>
<td>25</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>TSG-01a : Min Differential Output Voltage - Gen 1 LBP</td>
<td>57</td>
<td>0</td>
<td>46</td>
<td>2</td>
<td>103</td>
<td>2</td>
<td>98%</td>
</tr>
<tr>
<td>TSG-02a : Rise/Fall Time - Gen 1 rise</td>
<td>59</td>
<td>0</td>
<td>48</td>
<td>0</td>
<td>107</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>TSG-03a : Differential Skew - Gen 1 HFTP</td>
<td>12</td>
<td>0</td>
<td>8</td>
<td>0</td>
<td>20</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>TSG-04 : AC Common Mode Voltage</td>
<td>49</td>
<td>1</td>
<td>39</td>
<td>0</td>
<td>88</td>
<td>1</td>
<td>99%</td>
</tr>
<tr>
<td>TSG-05a : Rise/Fall Imbalance - HFTP TX+ r --&gt; TX- f</td>
<td>48</td>
<td>2</td>
<td>30</td>
<td>8</td>
<td>78</td>
<td>10</td>
<td>89%</td>
</tr>
<tr>
<td>TSG-06a: Amplitude Imbalance - HFTP</td>
<td>49</td>
<td>1</td>
<td>38</td>
<td>1</td>
<td>87</td>
<td>2</td>
<td>98%</td>
</tr>
<tr>
<td>TSG-09a : Gen 1 TJ @ Connector, Clock, f_{BAUD}/500 - HFTP</td>
<td>59</td>
<td>0</td>
<td>47</td>
<td>0</td>
<td>106</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>TSG-10a : Gen 1 DJ at Connector, Clock, f_{BAUD}/500 - HFTP</td>
<td>59</td>
<td>0</td>
<td>46</td>
<td>1</td>
<td>105</td>
<td>1</td>
<td>99%</td>
</tr>
<tr>
<td>TSG-11a : Gen 2 TJ at Connector, Clock, f_{BAUD}/500 - HFTP</td>
<td>45</td>
<td>5</td>
<td>37</td>
<td>2</td>
<td>82</td>
<td>7</td>
<td>92%</td>
</tr>
<tr>
<td>TSG-12a : Gen 2 DJ at Connector, Clock, f_{BAUD}/500 - HFTP</td>
<td>49</td>
<td>1</td>
<td>39</td>
<td>0</td>
<td>88</td>
<td>1</td>
<td>99%</td>
</tr>
<tr>
<td>RSG-01a: Gen1 Receive Jitter Test - 10 MHz</td>
<td>9</td>
<td>0</td>
<td>4</td>
<td>0</td>
<td>13</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>01b: 33 MHz</td>
<td>9</td>
<td>0</td>
<td>4</td>
<td>0</td>
<td>13</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>01c: 62 MHz</td>
<td>8</td>
<td>1</td>
<td>4</td>
<td>0</td>
<td>12</td>
<td>1</td>
<td>92%</td>
</tr>
<tr>
<td>01d: 5 MHz</td>
<td>8</td>
<td>1</td>
<td>4</td>
<td>0</td>
<td>12</td>
<td>1</td>
<td>92%</td>
</tr>
<tr>
<td>RSG-02a : Gen2 Receive Jitter Test</td>
<td>31</td>
<td>7</td>
<td>15</td>
<td>6</td>
<td>46</td>
<td>13</td>
<td>78%</td>
</tr>
<tr>
<td>02b: 33 MHz</td>
<td>32</td>
<td>6</td>
<td>16</td>
<td>5</td>
<td>48</td>
<td>11</td>
<td>81%</td>
</tr>
<tr>
<td>02c: 62 MHz</td>
<td>33</td>
<td>5</td>
<td>15</td>
<td>6</td>
<td>48</td>
<td>11</td>
<td>81%</td>
</tr>
<tr>
<td>02d: 5 MHz</td>
<td>33</td>
<td>5</td>
<td>16</td>
<td>5</td>
<td>49</td>
<td>10</td>
<td>83%</td>
</tr>
<tr>
<td>OOB-01a : OOB Signal Detection Threshold - Gen 1 ndet</td>
<td>24</td>
<td>0</td>
<td>12</td>
<td>1</td>
<td>36</td>
<td>1</td>
<td>97%</td>
</tr>
<tr>
<td>OOB-02 : UI During OOB Signaling</td>
<td>55</td>
<td>2</td>
<td>37</td>
<td>0</td>
<td>92</td>
<td>2</td>
<td>98%</td>
</tr>
<tr>
<td>OOB-03 : COMINIT/RESET and COMWake Transmit Burst Length</td>
<td>56</td>
<td>1</td>
<td>34</td>
<td>3</td>
<td>90</td>
<td>4</td>
<td>96%</td>
</tr>
<tr>
<td>OOB-04 : COMINIT/RESET Transmit Gap Length</td>
<td>57</td>
<td>0</td>
<td>34</td>
<td>3</td>
<td>91</td>
<td>3</td>
<td>97%</td>
</tr>
<tr>
<td>OOB-05 : COMWake Transmit Gap Length</td>
<td>54</td>
<td>3</td>
<td>34</td>
<td>3</td>
<td>88</td>
<td>6</td>
<td>94%</td>
</tr>
<tr>
<td>OOB-06a : COMWake Gap Detection Windows 103 det</td>
<td>55</td>
<td>3</td>
<td>35</td>
<td>1</td>
<td>90</td>
<td>4</td>
<td>96%</td>
</tr>
<tr>
<td>OOB-07a : COMINIT/RESET Gap Detection Windows - 306ns detect</td>
<td>58</td>
<td>0</td>
<td>36</td>
<td>1</td>
<td>94</td>
<td>1</td>
<td>99%</td>
</tr>
<tr>
<td>Test</td>
<td>IW#5 Pass</td>
<td>IW#5 Fail</td>
<td>IW#6 Pass</td>
<td>IW#6 Fail</td>
<td>Total Pass</td>
<td>Total Fail</td>
<td>Percent</td>
</tr>
<tr>
<td>---------------------------------</td>
<td>-----------</td>
<td>-----------</td>
<td>-----------</td>
<td>-----------</td>
<td>------------</td>
<td>------------</td>
<td>---------</td>
</tr>
<tr>
<td>GTR-01 : Software Reset</td>
<td>16</td>
<td>2</td>
<td>19</td>
<td>0</td>
<td>35</td>
<td>2</td>
<td>95%</td>
</tr>
<tr>
<td>GTR-02 : 3Gb/s Backwards Compatability</td>
<td>11</td>
<td>0</td>
<td>15</td>
<td>0</td>
<td>26</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>GTR-03 : DMA Protocol Support</td>
<td>16</td>
<td>2</td>
<td>18</td>
<td>1</td>
<td>34</td>
<td>3</td>
<td>92%</td>
</tr>
<tr>
<td>GTR-04 : Word 93 contents</td>
<td>18</td>
<td>0</td>
<td>17</td>
<td>2</td>
<td>35</td>
<td>2</td>
<td>95%</td>
</tr>
<tr>
<td>GTR-05 : Unrecognized FIS receipt</td>
<td>7</td>
<td>1.5</td>
<td>8.5</td>
<td>0.5</td>
<td>15.5</td>
<td>2</td>
<td>89%</td>
</tr>
<tr>
<td>NCQ-01 : Forced Unit Access</td>
<td>9</td>
<td>2</td>
<td>10</td>
<td>0</td>
<td>19</td>
<td>2</td>
<td>90%</td>
</tr>
<tr>
<td>NCQ-02 : Read Log Ext log page 10h support</td>
<td>12</td>
<td>0</td>
<td>9</td>
<td>0</td>
<td>21</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>NCQ-03 : Intermix of Legacy and NCQ commands</td>
<td>8</td>
<td>3</td>
<td>9</td>
<td>0</td>
<td>17</td>
<td>3</td>
<td>85%</td>
</tr>
<tr>
<td>NCQ-04 : Device response to malformed NCQ command</td>
<td>7</td>
<td>4</td>
<td>9</td>
<td>0</td>
<td>16</td>
<td>4</td>
<td>80%</td>
</tr>
<tr>
<td>NCQ-05 : DMA Setup Auto-Activate</td>
<td>9</td>
<td>1</td>
<td>9</td>
<td>0</td>
<td>18</td>
<td>1</td>
<td>95%</td>
</tr>
<tr>
<td>ASR-01 : COMINIT response interval</td>
<td>9</td>
<td>0</td>
<td>10</td>
<td>0</td>
<td>19</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>ASR-02 : COMINIT OOB interval</td>
<td>7</td>
<td>2</td>
<td>10</td>
<td>0</td>
<td>17</td>
<td>2</td>
<td>89%</td>
</tr>
<tr>
<td>ASR-03 : COMRESET OOB interval</td>
<td>4</td>
<td>2</td>
<td>6</td>
<td>3</td>
<td>10</td>
<td>5</td>
<td>67%</td>
</tr>
<tr>
<td>SSP-01 : Initialize Device Parameters</td>
<td>12</td>
<td>0</td>
<td>10</td>
<td>0</td>
<td>22</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>SSP-02 : Read/Write Stream Error Log</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>SSP-03 : Security Mode State</td>
<td>6</td>
<td>0</td>
<td>11</td>
<td>0</td>
<td>17</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>SSP-04 : Set Address Max</td>
<td>8</td>
<td>0</td>
<td>11</td>
<td>0</td>
<td>19</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>SSP-05 : Set Features – Write Cache Enable/Disable</td>
<td>10</td>
<td>0</td>
<td>10</td>
<td>0</td>
<td>20</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>SSP-06 : Set Features – Set Transfer Mode</td>
<td>13</td>
<td>1</td>
<td>17</td>
<td>1</td>
<td>30</td>
<td>2</td>
<td>94%</td>
</tr>
<tr>
<td>SSP-07 : Set Features – Advanced Power Management</td>
<td>4</td>
<td>0</td>
<td>5</td>
<td>0</td>
<td>9</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>SSP-08 : Set Features – Read Look-Ahead</td>
<td>10</td>
<td>0</td>
<td>10</td>
<td>0</td>
<td>20</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>SSP-11 : Set Multiple Mode</td>
<td>12</td>
<td>0</td>
<td>12</td>
<td>0</td>
<td>24</td>
<td>0</td>
<td>100%</td>
</tr>
<tr>
<td>IPM-01 : Partial State exit latency (host-initiated)</td>
<td>15</td>
<td>1</td>
<td>17</td>
<td>1</td>
<td>32</td>
<td>2</td>
<td>94%</td>
</tr>
<tr>
<td>IPM-02 : Slumber State exit latency (host-initiated)</td>
<td>15</td>
<td>1</td>
<td>19</td>
<td>0</td>
<td>34</td>
<td>1</td>
<td>97%</td>
</tr>
<tr>
<td>IPM-03 : Speed matching upon resume (host-initiated)</td>
<td>15</td>
<td>1</td>
<td>19</td>
<td>1</td>
<td>34</td>
<td>2</td>
<td>94%</td>
</tr>
<tr>
<td>IPM-04 : Lack of IPM support</td>
<td>6</td>
<td>1</td>
<td>6</td>
<td>0</td>
<td>12</td>
<td>1</td>
<td>92%</td>
</tr>
<tr>
<td>IPM-05 : Response to PMREQ_P</td>
<td>12</td>
<td>7</td>
<td>14</td>
<td>5</td>
<td>26</td>
<td>12</td>
<td>68%</td>
</tr>
<tr>
<td>IPM-06 : Response to PMREQ_S</td>
<td>12</td>
<td>7</td>
<td>15</td>
<td>6</td>
<td>27</td>
<td>13</td>
<td>68%</td>
</tr>
<tr>
<td>IPM-07 : Device default setting for device initiated requests</td>
<td>9</td>
<td>1</td>
<td>8</td>
<td>2</td>
<td>17</td>
<td>3</td>
<td>85%</td>
</tr>
<tr>
<td>IPM-08 : Device Initiated Power Management Enable</td>
<td>8</td>
<td>1</td>
<td>12</td>
<td>6</td>
<td>20</td>
<td>7</td>
<td>74%</td>
</tr>
<tr>
<td>IPM-09 : Partial State exit latency (device-initiated)</td>
<td>9</td>
<td>4</td>
<td>14</td>
<td>1</td>
<td>23</td>
<td>5</td>
<td>82%</td>
</tr>
<tr>
<td>IPM-10 : Slumber State exit latency (device-initiated)</td>
<td>11</td>
<td>2</td>
<td>6</td>
<td>0</td>
<td>17</td>
<td>2</td>
<td>89%</td>
</tr>
<tr>
<td>IPM-11 : Speed matching upon resume (device-initiated)</td>
<td>12</td>
<td>1</td>
<td>14</td>
<td>0</td>
<td>26</td>
<td>1</td>
<td>96%</td>
</tr>
</tbody>
</table>
Test Solution

- Interoperability Independent Test Lab

<table>
<thead>
<tr>
<th>Test Lab</th>
<th>Product Type</th>
<th>Supported Test Areas</th>
<th>Supported Interop Rev</th>
<th>Contact Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>Allion</td>
<td>Devices: HDD - 3.5&quot;, 2.5&quot; ODD - Half height ODD - Slim Hosts</td>
<td>Phy (PHY/TSB/OOB) RX/TX RSG Digital Mechanical System Interop</td>
<td>1.3 1.2 1.1* 1.0*</td>
<td>Allion Test Labs, Inc. Miss Jina Chen 9F, No. 3-1, Yuan Ku Street Taipei, Taiwan 11543, R.O.C. Tel: +886-2-7722-8800 Ext. 1855 Email: <a href="mailto:service@allion.com">service@allion.com</a> URL: <a href="http://www.allion.com">www.allion.com</a></td>
</tr>
</tbody>
</table>

- Approved MOI on Allion
  - Tektronix
  - Agilent
Interoperability Documentation v1.3

- SATA Interoperability Program Revision 1.3 - Policy Document v1.0
- SATA Interoperability Program Revision 1.3 - Unified Test Document v1.0

Additional test procedures and tool information is available for SATA-IO Member Download from the Logo WG Web page. Please log onto the Members Only area for access to these tests and document.

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Model</th>
<th>Ver</th>
<th>Date</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product Electrical 1.3 - PHY/TSG/OOB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Agilent</td>
<td>DSA91204A</td>
<td>1.0</td>
<td>6/12/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Tektronix</td>
<td></td>
<td>1.0</td>
<td>5/29/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>LeCroy</td>
<td></td>
<td>1.0</td>
<td>6/05/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Product Electrical 1.3 - RX/TX</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Agilent</td>
<td>86100C</td>
<td>1.0</td>
<td>10/13/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Tektronix</td>
<td>CSA8200</td>
<td>1.0</td>
<td>5/29/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Product Electrical 1.3 - RSG - 5 MHz, and eSATA signal level</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SyntheSys</td>
<td>7500B</td>
<td>1.0</td>
<td>12/18/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Tektronix</td>
<td>AWG7102/AWG7122B</td>
<td>1.0</td>
<td>5/22/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Agilent</td>
<td>N4903 J-BERT</td>
<td>1.0</td>
<td>5/29/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Device Digital 1.3 - GDR/NCQ/ASR/SSP/IPM - (updated IPM)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ulink</td>
<td></td>
<td>1.0 .1</td>
<td>9/27/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>LeCroy</td>
<td></td>
<td>1.0</td>
<td>2/19/2009</td>
<td>Approved</td>
</tr>
<tr>
<td>Host Digital 1.3 - ASR/IPM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ulink</td>
<td></td>
<td>1.0 .1</td>
<td>9/10/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>System Interop 1.3 - same as 1.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
SATA UTD V1.4 Information

Robert Liu

www.allion.com
• Naming Guidelines
• UTD 1.4 Overview
• Electronic Test Update
• Digital Test Update
• System Interoperability Test Update
• Equipment Renew
SATA Naming Guidelines

- Naming Guidelines

  - Please call this new specification by its proper name: Serial ATA International Organization: Serial ATA Revision 3.0

  - "SATA Revision 3.0" or "SATA 6Gb/s."
    - SATA 6Gb/s [product name]

  - Do not use the terms "SATA III" or "SATA 3.0,"

  - Do not use either "Third Generation" or "Gen3"
### SATA-IO Specifications and Naming Conventions

**Important:** Do not use the incorrect terms 'SATA II' or 'SATA III'
The references embedded within the SATA specifications to 'Gen 3', 'Gen 2', or 'Gen 1' are technical spec naming conventions only and should not be used for marketing and product naming purposes.

<table>
<thead>
<tr>
<th>Revision / Generation</th>
<th>Interface Name</th>
<th>Data Transfer Rate</th>
<th>Naming Convention</th>
</tr>
</thead>
<tbody>
<tr>
<td>SATA Revision 3.x (Not 'SATA III')</td>
<td>Third generation (not 'Gen 3')</td>
<td>Up to 6Gb/s</td>
<td>SATA 6Gb/s + [product name]</td>
</tr>
<tr>
<td>SATA Revision 2.x (Not 'SATA II')</td>
<td>Second generation (not 'Gen 2')</td>
<td>Up to 3Gb/s</td>
<td>SATA 3Gb/s + [product name]</td>
</tr>
<tr>
<td>SATA Revision 1.x (Not 'SATA I')</td>
<td>First generation (not 'Gen 1')</td>
<td>Up to 1.5Gb/s</td>
<td>SATA 1.5Gb/s + [product name]</td>
</tr>
</tbody>
</table>
### Overview of UTD 1.4 (Physical)

#### Phy Transmit Signal Requirements
- TSG-01: Differential Output Voltage
- TSG-02: Rise/Fall Time
- TSG-03: Differential Skew
- TSG-04: AC Common Mode Voltage
- TSG-05: Rise/Fall Imbalance
- TSG-06: Amplitude Imbalance
- TSG-07: Gen1 (1.5Gb/s) TJ at Connector, Clock to Data, fBAUD/10
- TSG-08: Gen1 (1.5Gb/s) DJ at Connector, Clock to Data, fBAUD/10
- TSG-09: Gen1 (1.5Gb/s) TJ at Connector, Clock to Data, fBAUD/500
- TSG-10: Gen1 (1.5Gb/s) DJ at Connector, Clock to Data, fBAUD/500
- TSG-11: Gen2 (3Gb/s) TJ at Connector, Clock to Data, fBAUD/500
- TSG-12: Gen2 (3Gb/s) DJ at Connector, Clock to Data, fBAUD/500
- TSG-13: Gen3 (6Gb/s) Transmit Jitter w/wo CIC
- TSG-14: Gen3 (6Gb/s) TX Maximum Differential Voltage Amplitude
- TSG-15: Gen3 (6Gb/s) TX Minimum Differential Voltage Amplitude
- TSG-16: Gen3 (6Gb/s) Tx AC Common Mode Voltage

#### Phy Receive Signal Requirement
- RSG-01: Gen1 (1.5Gb/s) Receiver Jitter Tolerance Test (Normative)
- RSG-02: Gen2 (3Gb/s) Receiver Jitter Tolerance Test (Normative)
- RSG-03: Gen3 (6Gb/s) Receiver Jitter Tolerance Test
- RSG-05: Gen1 Asynchronous Receiver Stress Test at +350ppm
- RSG-06: Gen1 Asynchronous Receiver Stress Test With SSC

#### SI General Requirements
- SI-1.8: Cable Characterization
- SI-09: Inter-Symbol Interference

#### Phy General Requirements
- PHY-01: Unit Interval
- PHY-02: Frequency Long Term Stability
- PHY-03: Spread-Spectrum Modulation Frequency
- PHY-04: Spread-Spectrum Modulation Deviation

#### Phy OOB Requirements
- OOB-01: OOB Signal Detection Threshold
- OOB-02: UI During OOB Signaling
- OOB-03: COMINIT/RESET and COMWAKE Transmit Burst Length
- OOB-04: COMINIT/RESET Transmit Gap Length
- OOB-05: COMWAKE Transmit Gap Length

#### Phy Receiver/Transmitter Channel Reqs
- RX/TX-01: Pair Differential Impedance
- RX/TX-02: Single-Ended Impedance (Obsolete)
- RX/TX-03: Gen2 (3Gb/s) Differential Mode Return Loss
- RX/TX-04: Gen2 (3Gb/s) Common Mode Return Loss
- RX/TX-05: Gen2 (3Gb/s) Impedance Balance
- RX/TX-06: Gen1 (1.5Gb/s) Differential Mode Return Loss
- RX/TX-07: Gen3 (6Gb/s) Differential Mode Return Loss
- RX/TX-08: Gen3 (6Gb/s) Impedance Balance

#### SATA Measurement Legends:
- No change from previous UTD 1.3 spec version
- Revised methodology from UTD1.3 to UTD 1.4
- New test definitions in UTD 1.4
- Obsolete
### Overview of UTD 1.4 (Digital)

<table>
<thead>
<tr>
<th>General Test Requirements</th>
<th>Software Settings Preservation</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTR-01 : Software Reset</td>
<td>SSP-01 : Initialize Device Parameters</td>
</tr>
<tr>
<td>GTR-02 : SATA Gen-2 or above Signaling Speed Backwards Compatibility</td>
<td>SSP-02 : Read/Write Stream Error Log</td>
</tr>
<tr>
<td>GTR-03 : DMA Protocol Support</td>
<td>SSP-03 : Security Mode State</td>
</tr>
<tr>
<td>GTR-04 : General SATA Support</td>
<td>SSP-04 : Set Address Max</td>
</tr>
<tr>
<td>GTR-05 : Unrecognized FIS receipt (Informative)</td>
<td>SSP-05 : Set Features – Write Cache Enable/Disable</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Native Command Queuing</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>NCQ-01 : Forced Unit Access</td>
<td>SSP-06 : Set Features – Set Transfer Mode</td>
</tr>
<tr>
<td>NCQ-02 : Read Log Ext log page 10h support</td>
<td>SSP-07 : Set Features – Advanced Power Management Enable/Disable</td>
</tr>
<tr>
<td>NCQ-03 : Intermix of Legacy and NCQ commands</td>
<td>SSP-08 : Set Features – Read Look-Ahead</td>
</tr>
<tr>
<td>NCQ-04 : Device response to malformed NCQ command</td>
<td>SSP-09 : Set Features – Release Interrupt</td>
</tr>
<tr>
<td>NCQ-05 : DMA Setup Auto-Activate</td>
<td>SSP-10 : Set Features – Service Interrupt</td>
</tr>
<tr>
<td>NCQ-06 : Forced Unit Access</td>
<td>SSP-11 : Set Multiple Mode</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Digital Optional Features</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DOF-01 : Asynchronous notification</td>
<td></td>
</tr>
<tr>
<td>DOF-02 : Phy speed indicator</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Software Settings Preservation</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SSP-01 : Initialize Device Parameters</td>
<td>IPM-01 : Partial State exit latency (host-initiated)</td>
</tr>
<tr>
<td>SSP-02 : Read/Write Stream Error Log</td>
<td>IPM-02 : Slumber State exit latency (host-initiated)</td>
</tr>
<tr>
<td>SSP-03 : Security Mode State</td>
<td>IPM-03 : Speed matching upon resume (host-initiated)</td>
</tr>
<tr>
<td>SSP-04 : Set Address Max</td>
<td>IPM-04 : NAK of requests when support not indicated</td>
</tr>
<tr>
<td>SSP-05 : Set Features – Write Cache Enable/Disable</td>
<td>IPM-05 : Response to PMREQ_P</td>
</tr>
<tr>
<td>SSP-06 : Set Features – Set Transfer Mode</td>
<td>IPM-06 : Response to PMREQ_S</td>
</tr>
<tr>
<td>SSP-07 : Set Features – Advanced Power Management Enable/Disable</td>
<td>IPM-07 : Device default setting for device initiated requests</td>
</tr>
<tr>
<td>SSP-08 : Set Features – Read Look-Ahead</td>
<td>IPM-08 : Device Initiated Power Management enable / disable</td>
</tr>
<tr>
<td>SSP-09 : Set Features – Release Interrupt</td>
<td>IPM-09 : Partial State exit latency (device-initiated)</td>
</tr>
<tr>
<td>SSP-10 : Set Features – Service Interrupt</td>
<td>IPM-10 : Slumber State exit latency (device-initiated)</td>
</tr>
<tr>
<td>SSP-11 : Set Multiple Mode</td>
<td>IPM-11 : Speed matching upon resume (device-initiated)</td>
</tr>
<tr>
<td>SSP-12 : Set Features – Write-Read-Verify</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Interface Power Management</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>IPM-04 : NAK of requests when support not indicated</td>
<td></td>
</tr>
<tr>
<td>IPM-05 : Response to PMREQ_P</td>
<td></td>
</tr>
<tr>
<td>IPM-06 : Response to PMREQ_S</td>
<td></td>
</tr>
<tr>
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<td></td>
</tr>
<tr>
<td>IPM-09 : Partial State exit latency (device-initiated)</td>
<td></td>
</tr>
<tr>
<td>IPM-10 : Slumber State exit latency (device-initiated)</td>
<td></td>
</tr>
<tr>
<td>IPM-11 : Speed matching upon resume (device-initiated)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Asynchronous Signal Recovery</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ASR-01 : COMINIT response interval</td>
<td></td>
</tr>
<tr>
<td>ASR-02 : COMINIT OOB Interval</td>
<td></td>
</tr>
<tr>
<td>ASR-03 : COMRESET OOB Interval</td>
<td></td>
</tr>
</tbody>
</table>

Legends:
- No change from previous UTD 1.3 spec version
- Revised methodology from UTD1.3 to UTD 1.4
- New test definitions in UTD 1.4
**Electronic Tests Update**

- **Electronic Test**
  - Receiver Jitter Tolerance Test
    - The device need to run the applicable RSG tests.
    - Ex: SATA 6.0Gb/s: RSG-01, RSG-02 and RSG-03

<table>
<thead>
<tr>
<th>Test pattern setup file for RSG-01: Normative, Required for all PUTs. AWG7000 SATA- RSG-01_V1_4Compliance.zip</th>
<th>SATA usage model: 1.5Gbps(Gen1i)</th>
<th>Test time/PJ freq waveform</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>RSG01a 10Mhz 10 Min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RSG01b 33Mhz 10 Min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RSG01c 62Mhz 10 Min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RSG01d 5Mhz 10 Min</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test pattern setup file for RSG-02: Normative, Required for PUTs claiming ability to run Gen2i and Gen3i rates. AWG7000 SATA- RSG-02_V1_4Compliance.zip</th>
<th>SATA usage model: 3Gbps(Gen2i) + 0ppm</th>
<th>Test time/PJ freq waveform</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>RSG02a 10Mhz 5 Min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RSG02b 33Mhz 5 Min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RSG02c 62Mhz 5Min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RSG02d 5Mhz 5 Min</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test pattern setup file for RSG-03: Informative, Required for PUTs claiming ability to run Gen3i rates. AWG7122B SATA- RSG-03_V1_4Compliance.zip</th>
<th>SATA usage model: 6Gbps(Gen3i) +0ppm</th>
<th>Test time/PJ freq waveform</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>RSG03a 10Mhz 2.5 Min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RSG03b 33Mhz 2.5 Min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RSG03c 62Mhz 2.5 Min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RSG03d 5Mhz 2.5 Min</td>
</tr>
</tbody>
</table>
Electronic Tests Update

- Electronic Test
  - Receiver Jitter Tolerance Test
    - Receiver Stress Test at +350ppm (Informative)
      - Data Rate of the pattern generator: 1.5Gb/s + 350ppm
      - No more than 0 frame errors over minimum of 18 successive iterations framed COMP pattern
    - Receiver Stress with SSC (Informative)
      - Data Rate range is between 1.5Gb/s – 5350ppm and 1.5Gb/s - 350ppm
      - No more than 0 frame errors over minimum of 18 successive iterations framed COMP pattern
Electronic Tests Update

- General RSG Calibration
  - TP1: Rise/Fall time, Rj, Sj,
  - TP2: Tj, Amplitude

Figure 1 – Test points for RSG setup calibration.
Digital Tests Update

• Digital Test

  – Multiple Signaling Speed establish
    • DUT need to verify compatible speed

  – New Test
    • Asynchronous Notification
      – A mechanism for a device to send a notification to the host the device requires attention
    • PHY Speed Indicator
      – Check the interface rate is equal to IDENTIFY DEVICE or IDENTIFY PACKET DEVICE info.
System Interoperability Tests Update

- System Interoperability
  - Test OS
    - May upgrade from Dos to Windows
  - Test Tool
    - Dos: HP Dos tool
    - Windows: Ulink DriveMaster
• System Interoperability

  – for Device
    • 5 Gold systems
    • At least 3 different SATA chipset
    • At least 2 6Gb/s system
    • At least 1 6Gb/s system support SSC on

  – for Host
    • 5 Gold devices
    • At least 2 6Gb/s devices
    • At least 1 6Gb/s device support SSC on
    • 2 ODD Devices
    • At least 1 ODD support SSC on
**Equipment Renew**

**Electronic**
- RSG / Frame Error Counter
  - SATA 1.5Gb/s & SATA 3Gb/s: Crescent Heart Frame Error Counter
  - SATA 6Gb/s: Finisar Xgig or SerialTek BusXpert Micro Analyzer
- RSG / CIC Channel
  - Tektronix: AWG
  - Agilent: ISI Board

**Digital**
- Bus Analyzer
  - SATA 1.5Gb/s & SATA 3Gb/s: LeCroy CATC
  - SATA 6Gb/s: Finisar Xgig, SerialTek BusXpert Micro Analyzer, LeCroy Sierra M6 or STX-460
- Test Software
  - DriveMaster 2010
Thank You

Session Break

3:00~3:20

Coming Up:

SATA Certified Logo Process

Jina Chen
SATA Certified Logo Process

An ISO/IEC 17025 Qualified Test Laboratory

Jina Chen

www.allion.com

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Agenda

- SATA certified logo Introduction
- SATA Certified Logo Overall Process
- Retest Policy
Who is eligible to use the SATA certified logos?

Only devices that are passed the SATA Interoperability test and shown on the Integrators List (IL) are eligible to use the SATA Certified Logo.
The first step is to become a SATA member.

http://www.serialata.org/membership/join_sataio.asp

US$1,700 annual membership

For non SATA-IO member, US$1,000 fee would be charged per IL listing of product/family

In addition to the $1,000 fee per IL listing, non SATA-IO members will need to pay US$750 per product for the right to use the Certified Logos.
# SATA certified logo Introduction – Become a SATA Member

<table>
<thead>
<tr>
<th></th>
<th>Annual Fee</th>
<th>IL listing</th>
<th>The right to use the Certified Logos</th>
</tr>
</thead>
<tbody>
<tr>
<td>SATA-IO Members</td>
<td>US$1,700/per year</td>
<td>Free</td>
<td>Free</td>
</tr>
<tr>
<td>Non SATA-IO Members</td>
<td>NA</td>
<td>US$1,000/per product</td>
<td>US $750/ per product</td>
</tr>
</tbody>
</table>
SATA certified logo Introduction –
The difference between SATA Logos

- SATA-IO Logos to Indicate SATA-IO Membership (Member Only)

- Certified Logo
**SATA Certified Logo Overall Process**

1. **Vendor Contact**
   - Allion to Request the test

2. **Vendor Prepare the Samples and Documents**

3. **Testing at Allion**

4. **Allion Send the Report to the Vendor**

5. **SATA-IO Review**
   - The result then put device on the Integrator List

6. **Allion Request TID and Submit Result to SATA-IO for Review**

7. **If PASS**
   - Allion send the pass notification to vendor
   - Vender request SATA-IO if the product need to carry certified logo
   - SATA-IO review the request and will send the logo to the vendor

8. **Vendor Contact**
   - Allion to Request the test

9. **Vendor Prepare the Samples and Documents**

10. **Testing at Allion**

11. **Allion Send the Report to the Vendor**

12. **SATA-IO Review**
    - The result then put device on the Integrator List

13. **Allion Request TID and Submit Result to SATA-IO for Review**

14. **If PASS**
    - Allion send the pass notification to vendor
    - Vender request SATA-IO if the product need to carry certified logo
    - SATA-IO review the request and will send the logo to the vendor
SATA Certified Logo Overall Process

1. Vendor Contact
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   The result then put device on the Integrator List
   If PASS

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7. Vender request SATA-IO if the product need to carry certified logo

8. SATA-IO review the request and will send the logo to the vendor

9. Allion send the pass notification to vender
Interoperability Independent Test Labs

It is now possible to have your product tested in independent laboratories. You will first need to review the following information.

The testing performed by the independent test labs is consistent with the tests executed at a Serial ATA Interoperability Workshop. Vendors may contact the test labs directly to understand which Methods of Implementation (MOIs) are approved for the appropriate lab. To obtain the latest revision of a specific MOI as well as the test requirements documentation (Unified Test Document, please visit the Interoperability Documentation web page).

A high level description of the product and testing submission process can be obtained here.

Check to see which labs are available to test your product. Testing requests to SATA-Io qualified independent laboratories are handled directly by the test labs themselves. The test labs are responsible for the appropriate coordination with SATA-Io regarding testing status and results submission.

<table>
<thead>
<tr>
<th>Test Lab</th>
<th>Product Type</th>
<th>Supported Test Areas</th>
<th>Supported Interop Rev</th>
<th>Contact Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>Allion</td>
<td>Devices: HDD - 3.5&quot;, 2.5&quot; HDD - Half height ODD - Slim Hosts</td>
<td>Phy (PHY/TSB/OOB) R/X/TX RSG Digital Mechanical System Interop</td>
<td>1.3 1.2 1.1* 1.0*</td>
<td>Allion Test Labs, Inc. Miss Jina Chen 9F, No. 3-1, Yuan Ku Street Taipei, Taiwan 11543, R.O.C. Tel: +886-2-7722-8800 Ext. 1855 Email: <a href="mailto:service@allion.com">service@allion.com</a> URL: <a href="http://www.allion.com">www.allion.com</a></td>
</tr>
</tbody>
</table>
Vendor Contact
Allion to Request
the test

Vendor Prepare
the Samples
and Documents

Testing at Allion

Testing at Allion

Allion Send
the Report
to the Vendor

SATA-IO Review
The result then put device on the Integrator List

Allion Request TID and Submit Result to SATA-IO for Review

If PASS

Allion send the pass notification to vendor

Vender request SATA-IO if the product need to carry certified logo

SATA-IO review the request and will send the logo to the vendor
Prepare the Samples and Documents

• Test Requirement
  – Prepare 2 samples for testing
  – Fill out the information form
  – Fill out the submission form
Serial ATA Test Report
For
Gen2 Device

Company Name:
Model Name:
Hardware Revision:
Firmware Revision:
Product Type: Please Select One

Product Receive Date: mm/dd/yyyy
Test Start Date: mm/dd/yyyy
Report Date: mm/dd/yyyy
Test Result: Please Select One

Company Name:
Company Address:
Technical Contact:
Name:
Phone Number:
E-Mail:
FAX Number:
Marketing Contact:
Name:
Phone Number:
E-Mail:
FAX Number:
<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>I</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Serial ATA</td>
<td>SATA-IO Interoperability Testing</td>
<td>Rev 1.3 [A10]</td>
<td>INCOMPLETE</td>
<td>List Link</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Interop Workshop #/Test Lab</td>
<td>Allion, Taiwan</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Product Test ID (TID):</td>
<td>4</td>
<td>*</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Product Type:</td>
<td>4</td>
<td>*</td>
<td></td>
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</tr>
</tbody>
</table>

**Product Capabilities** (all questions must be answered)

- Does your product support (Y/N):
  - Native Command Queuing (Y/N)? * NCQ
  - Asynchronous Signal Recovery (Y/N)? * ASR
  - Software Settings Preservation (Y/N)? * SSP
  - Interface Power Management (device initiated) (Y/N)? * IPMd
  - Interface Power Management (host initiated) (Y/N)? * IPMh
  - 3Gb/s Interface Rate (Y/N)? * 3Gb/s
  - Spread Spectrum Clocking (SSC) (Y/N)? * SSC
  - If SSC is supported, can it be turned ON/OFF (Y/N)?

Select “Allion, Taiwan”

Leave Blank if not retest submission

Required fields
<table>
<thead>
<tr>
<th>Question</th>
<th>Answer Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>Is this a retest or update submission (Y/N)?</td>
<td>If yes, retest section required</td>
</tr>
<tr>
<td>Is this a product family submission (Y/N)?</td>
<td>If yes, retest AND product family section required</td>
</tr>
<tr>
<td>Is this a Single family listing (Y/N)?</td>
<td>If yes, retest AND single family listing section required</td>
</tr>
<tr>
<td>Do you plan to release this product to the public market &lt; 6 months from now (Y/N)?</td>
<td>If NO, please comment:</td>
</tr>
<tr>
<td>Do you plan to make any significant hardware or firmware changes to your product after testing that will affect SATA compatibility or functionality (Y/N)?</td>
<td>If YES, please comment:</td>
</tr>
<tr>
<td>If your product successfully completes Interop Testing, would you like to have your product IMMEDIATELY listed on the SATA-IO Integrators List (Y/N)?</td>
<td>If NO, please comment (i.e. never or delay until notified by the product vendor):</td>
</tr>
</tbody>
</table>
If more than 10 specific Family models then request single family Listing (general family listing) wildcard characters such as X or * or # can be used.
**SATA Certified Logo Overall Process**

- **Vendor Contact**
  - Allion to Request the test

- **Vendor Prepare**
  - the Samples and Documents

- **Testing at Allion**

- **SATA-IO Review**
  - The result then put device on the Integrator List

- **Allion Request TID and Submit Result to SATA-IO for Review**

- **Allion Send the Report to the Vendor**

  - If PASS:
    - Allion send the pass notification to vendor
    - Vender request SATA-IO if the product need to carry certified logo
    - SATA-IO review the request and will send the logo to the vendor
• **Test Schedule**
  – 3 working days with 2 samples are provided

• **Testing Sample Keep**
  – The product sample which was used in the testing will be kept for at least 6 months.
SATA Certified Logo Overall Process

Vendor Contact
Allion to Request the test

Vendor Prepare the Samples and Documents

Testing at Allion

Allion Send the Report to the Vendor

If PASS:

SATA-IO Review
The result then put device on the Integrator List

Allion Request TID and Submit Result to SATA-IO for Review

Vender request SATA-IO if the product need to carry certified logo

SATA-IO review the request and will send the logo to the vender

Allion send the pass notification to vender
SATA Certified Logo Overall Process

Vendor Contact Allion to Request the test

Vendor Prepare the Samples and Documents

Testing at Allion

Stata-IO Review The result then put device on the Integrator List

Allion Request TID and Submit Result to SATA-IO for Review

If PASS

Allion Send the Report to the Vendor

Allion send the pass notification to vendor

Vender request SATA-IO if the product need to carry certified logo

SATA-IO review the request and will send the logo to the vendor
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If PASS

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SATA-IO Review
The result then put device on the Integrator List

SATA-IO review the request and will send the logo to the vender

Vender request SATA-IO if the product need to carry certified logo

Allion send the pass notification to vendor
The Integrators List (IL) is a database on the SATA-IO website which includes information about the components that have passed the Serial ATA Interoperability testing. [http://www.serialata.org/developers/integrators_list.asp](http://www.serialata.org/developers/integrators_list.asp)

<table>
<thead>
<tr>
<th>HDD</th>
<th>Details</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>E Series SSD</strong></td>
<td>Model: E80, E150, E320, EA0080X-XXXXX-XX-XX, EA0160X-XXXXX-XX-XX, EA0320X-XXXXXX-XX-XX</td>
<td>Features: 3Gb/s, SSP, ASR, IPMh/</td>
</tr>
<tr>
<td>Made by: Entorian Technologies</td>
<td>Test ID: 002020201 / Interop Level: 1.2</td>
<td></td>
</tr>
<tr>
<td>Contact: email / website</td>
<td>Date Listed: 12/30/2009</td>
<td></td>
</tr>
</tbody>
</table>

| Deskstar, CinemaStar | Model: HDP7250xxxxxxx, HCP7250xxxxxxx | Features: SSC, NCQ, 3Gb/s, SSP, ASR, JPMd, IPMh | Part #: Deskstar P7K500, CinemaStar P7K500 |
| Made by: Hitachi | Test ID: 002020083 / Interop Level: 1.2 |                                               |
| Contact: email / website | Revision: 0214e10 |                                               |
| Date Listed: 1/7/2008 |                                      |                                               |

| Travelstar | Model: HTS5450xxxxxxx, HTE5450xxxxxxx | Features: SSC, NCQ, 3Gb/s, SSP, ASR, JPMd, IPMh | Part #: Travelstar 5K500, Travelstar E5K500 |
| Made by: Hitachi | Test ID: 001020091 / Interop Level: 1.2 |                                               |
| Contact: email / website | Revision: C60B |                                               |
| Date Listed: 1/6/2008 |                                      |                                               |

| Travelstar, CinemaStar | Model: HTS5432xxxxxxx, HTE5432xxxxxxx, HCC5432xxxxxxx | Features: SSC, NCQ, 3Gb/s, SSP, ASR, JPMd, IPMh | Part #: Travelstar 5K320, CinemaStar C5K320 |
| Made by: Hitachi | Test ID: 002020104 / Interop Level: 1.2 |                                               |
| Contact: email / website | Revision: C30C |                                               |
| Date Listed: 2/29/2008 |                                      |                                               |

| Travelstar | Model: HTx5460xxB9xxxxx, HCC5460xxB9xxxxx | Features: SSC, NCQ, 3Gb/s, SSP, ASR, JPMd, IPMh | Part #: Travelstar 5K500, B, CinemaStar C5K500 |
| Made by: Hitachi | Test ID: 002020177 / Interop Level: 1.2 |                                               |
| Contact: email / website | Revision: x |                                               |
| Date Listed: 10/24/2008 |                                      |                                               |
SATA Certified Logo Overall Process

1. **Vendor Contact**
   - Allion to Request the test

2. **Vendor Prepare**
   - the Samples and Documents

3. **Testing at Allion**

4. **SATA-IO Review**
   - The result then put device on the Integrator List

5. **Allion Request TID**
   - and Submit Result to SATA-IO for Review

6. **Allion Send the Report to the Vendor**
   - If PASS

7. **Allion send the pass notification to vendor**

8. **Vendor request SATA-IO if the product need to carry certified logo**

9. **SATA-IO review the request and will send the logo to the vendor**
Dear XX,

Your SSD product was tested with test ID (TID) #XXX by Allion, a SATA-IO certified test lab. This email will clarify the assessment of your product based on the defined testing for the Interoperability Program, and provide the assessment of your product for listing on the Integrators List based on test results obtained by Allion.

Approved for Integrators List: Yes
Capabilities Approved:
- Asynchronous Signal Recovery

Notes: PHY-01, TSG-01, TSG-02, and RX-06 values are within 5% of allowed limit. We have concerns about these parameters staying within their respective passing ranges over the variances of normal manufacturing processes.

Applicable Interop Program Revision: 1.2
Congratulations, your product with TID #XXX has been listed on the SATA-IO Integrators List based on the information provided to Allion. Please review your product listing at www.sata-io.org/developers/integrators_list.asp and let us know if any additional changes are needed.

Certified Logo Program Approved:
Your product is now eligible to use the certified SATA logos. In order to use the certified logos, each company must sign the Certification Mark License Agreement. Only devices that are shown on the Integrators List are eligible for the Certified Logo program. If your company would like to use the certified logos to help promote its approved products, please contact SATA-IO and we will send the License Agreement for your company's authorized signature authority to sign. There is no cost to SATA-IO Member companies to use the certified SATA logos.

The test results gathered from Allion are attached. Please feel free to contact SATA-IO Administration (admin@sata-io.org) with any questions.
How to receive the certified logos

- Once your product has passed Interoperability Testing and is listed on the Integrators List, you will receive an email from Allion announcing that your product has passed.

- Your company must sign the Certified Logo License Agreement, which will be provided by SATA-IO.

- Once the signed agreement has been received by SATA-IO, and SATA-IO has verified that your products are on the Integrators List, the certified logos will be sent to you.

Only devices that are **shown on the Integrators List** are eligible for the Certified Logo program.
SATA Certified Logo Overall Process

Vendor Contact Allion to Request the test

Vendor Prepare the Samples and Documents

Testing at Allion

Allion Send the Report to the Vendor

SATA-IO Review The result then put device on the Integrator List

Allion Request TID and Submit Result to SATA-IO for Review

If PASS

Vender request SATA-IO if the product need to carry certified logo

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Allion send the pass notification to vender
Vendor Contact Allion to Request the test
Vendor Prepare the Samples and Documents
Testing at Allion
Allion Send the Report to the Vendor
Allion Request TID and Submit Result to SATA-IO for Review
SATA-IO review the request and will send the logo to the vendor
SATA-IO send the pass notification to vendor
Vendor request SATA-IO if the product need to carry certified logo
SATA-IO Review The result then put device on the Integrator List
If PASS:

Vender request SATA-IO if the product need to carry certified logo
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SATA-IO send the pass notification to vendor
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SATA-IO send the pass notification to vendor
Vendor request SATA-IO if the product need to carry certified logo
SATA-IO Review The result then put device on the Integrator List
If PASS:
Retest Policy

• Link: http://www.sata-io.org/developers/interop_13.asp

Interoperability Documentation v1.3

  - SATA Interoperability Program Revision 1.3 - Policy Document v1.0
  - SATA Interoperability Program Revision 1.3 - Unified Test Document v1.0

Additional test procedures and test information is available for SATA-IO Member Download page. Please log onto the Members Only area for access to these tests and document.

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Model</th>
<th>Ver</th>
<th>Date</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product Electrical 1.3 - PHY/TSG/00B</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Agilent</td>
<td>DSA91204A</td>
<td>1.0</td>
<td>6/12/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Tektronix</td>
<td>1.0</td>
<td>5/29/2008</td>
<td>Approved</td>
<td></td>
</tr>
<tr>
<td>LeCroy</td>
<td>1.0</td>
<td>6/05/2008</td>
<td>Approved</td>
<td></td>
</tr>
<tr>
<td>Product Electrical 1.3 - RX/TX</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Agilent</td>
<td>86100C</td>
<td>1.0</td>
<td>10/13/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Tektronix</td>
<td>1.0</td>
<td>5/29/2008</td>
<td>Approved</td>
<td></td>
</tr>
<tr>
<td>Product Electrical 1.3 - RSG - 5 MHz, and eSATA signal level</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SyntheSys</td>
<td>7500E</td>
<td>1.0</td>
<td>12/10/2000</td>
<td>Approved</td>
</tr>
<tr>
<td>Tektronix</td>
<td>AWG7102/AWG7122B</td>
<td>1.0</td>
<td>5/22/2008</td>
<td>Approved</td>
</tr>
<tr>
<td>Agilent</td>
<td>N4903 3-BERT</td>
<td>1.0</td>
<td>5/29/2008</td>
<td>Approved</td>
</tr>
</tbody>
</table>
Retest Policy

- See Section 4.4 of the policy document

<table>
<thead>
<tr>
<th>Change Type</th>
<th>Product Type</th>
<th>Re-Test form and Action required</th>
</tr>
</thead>
<tbody>
<tr>
<td>Longer or shorter cable length not already tested in previous family testing</td>
<td>Cable</td>
<td>Run complete cable electrical tests</td>
</tr>
<tr>
<td>Connector construction (orientation angle, crimp vs solder, physical size)</td>
<td>Cable</td>
<td>Run complete cable electrical &amp; mechanical tests</td>
</tr>
<tr>
<td>No material SATA change – different vendor or model #, bezel color, capacity.</td>
<td>Device/Host</td>
<td>No re-testing required.</td>
</tr>
<tr>
<td>Additional source of connector, PCB or support components (AC caps, etc)</td>
<td>Device/Host</td>
<td>No re-testing required IF additional source has the same characteristics and does not cause a PCB layout change. Shall declare same characteristics on Re-test form</td>
</tr>
<tr>
<td>Connector</td>
<td>Device/Host</td>
<td>Run PHY/TSG/OOB/RSG, RX/TX, System Interop and applicable MDx or MHx tests</td>
</tr>
<tr>
<td>PCB SATA layout, stack up, geometry or material type</td>
<td>Device/Host</td>
<td>Run PHY/TSG/OOB/RSG, RX/TX, System Interop tests</td>
</tr>
<tr>
<td>SATA interface silicon</td>
<td>Device/Host</td>
<td>Run PHY/TSG/OOB/RSG, RX/TX, Digital, System Interop tests</td>
</tr>
<tr>
<td>SATA interface non-silicon parts (AC caps, etc)</td>
<td>Device/Host</td>
<td>Run PHY/TSG/OOB/RSG, RX/TX, System Interop tests</td>
</tr>
<tr>
<td>Firmware – SATA interface impact (SSC, signal level, edge rate, etc)</td>
<td>Device/Host</td>
<td>Run PHY/TSG/OOB/RSG, RX/TX, System Interop tests</td>
</tr>
<tr>
<td>Firmware – Link layer (DIPM, etc)</td>
<td>Device/Host</td>
<td>Run Digital, System Interop tests</td>
</tr>
<tr>
<td>Firmware – New or changed SATA Feature sets (NCQ, etc)</td>
<td>Device/Host</td>
<td>Run Digital, System Interop tests</td>
</tr>
<tr>
<td>Firmware – Removal of optional SATA</td>
<td>Device/Host</td>
<td>No re-testing required</td>
</tr>
</tbody>
</table>
Retest Policy

• Requirement depends on the changed level

• If the change impacts SATA function:
  (1) Contact Allion to perform the partial test
  (2) Fill out the submission document (especially retest part)
  (3) After the test is finished, Allion will submit the result to SATA-IO for reviewing.
  (4) After the review process is done, the Integrator List will be updated by SATA-IO.
### Retest Policy

#### Test Results from Previous Product

- **Must explain why test results from the previous product can be used.**

<table>
<thead>
<tr>
<th>Test Type</th>
<th>Question</th>
<th>Option</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>SATA Impacting Changes</td>
<td>Are there any SATA impacting material changes or difference between products (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>New Source of Connector</td>
<td>New source of connector, PCB or SATA support components (AC caps, etc) (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>Connector Change</td>
<td>Connector change in design or requirements or different between products (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>If Y</td>
<td>If &quot;Y&quot;, PHY/TSG/OOB, RX/TX, and MDI tests results included (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>PCB Change</td>
<td>PCB change or different (SATA layout, stack up, geometry or material type) (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>If Y</td>
<td>If &quot;Y&quot;, PHY/TSG/OOB and RX/TX test results included (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>SATA Interface Silicon</td>
<td>SATA interface silicon change or different (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>If Y</td>
<td>If &quot;Y&quot;, PHY/TSG/OOB and RX/TX test results included (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>SATA Interface Parts</td>
<td>SATA interface non-silicon parts change or different (AC caps, etc) (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>If Y</td>
<td>If &quot;Y&quot;, PHY/TSG/OOB and RX/TX test results included (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>Firmware Change</td>
<td>Firmware change or different - SATA interface impact (SSC, signal level, edge rate) (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>If Y</td>
<td>PHY/TSG/OOB and RX/TX test results included (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>Firmware Change</td>
<td>Firmware change or different - Link layer (DIPM, etc) (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>Digital Test Results</td>
<td>Digital test results included (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>Firmware Change</td>
<td>Firmware change or different - Removal of optional SATA feature (Y/N)</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>Firmware Change</td>
<td>Firmware change or different - Non-SATA impacting (additional media vendor support) (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>External Material</td>
<td>External material changes or differences (change in size or shape of exterior) (Y/N)?</td>
<td>Y/N</td>
<td></td>
</tr>
<tr>
<td>All Other Test Results</td>
<td>Why are all other test results still valid or all applicable to all products of family?</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
• SATA-IO Website  
http://www.serialata.org/

• How to join SATA-IO member  
http://www.serialata.org/membership/join_sataio.asp

• SATA-IO Interoperability Testing Information  
http://www.serialata.org/developers/interoperability.asp

• Certified Logo Program Information  
http://www.serialata.org/developers/certified_logo_program.asp
Thank You

Coming Up:
SATA SSD Testing

Richard Shen
• Interoperability Test
• OS Independent Test
Interoperability Test

System compatibility Test
- BIOS Enumeration
  - AHCI Mode
  - IDE Mode
Interoperability Test

System compatibility Test

• System Installation
  Ÿ Different File Format (FAT32, NTFS, Ext and Apple HFS Plus)
  Ÿ Device Enumeration
  Ÿ File IO and File Compare
  Ÿ Power Management Test
  Ÿ Hot Plug/ Unplug Test
Interoperability Test

RAID Controller Compatibility Test
(On Board Chipset and Add on Card)

- RAID 0
- RAID 1
- RAID 5
- RAID 0+1
- Other
Interoperability Test

Enclosure Test

- Enclosure Type (USB, E-SATA, 1394 and Ethernet)
- Capability with variety Operation system (Windows, Apple Mac and Linux)
  - Device Enumeration
  - File IO and File Compare
  - Power Management Test
  - Hot Plug/ Unplug Test
Interoperability Test

Performance Test
• HD Tune
• FDBENCH
• PCMark
• HDTachRW
• Iometer
## Interoperability Test

### HD Tune 2.55

<table>
<thead>
<tr>
<th>Product</th>
<th>Burst Rate (MB/sec)</th>
<th>Average (MB/sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SanDisk SDS5C-032G-102500 A-3.13</td>
<td>58.7</td>
<td>64.5</td>
</tr>
<tr>
<td>SAMSUNG_MCBQE64GBMPP-03A 64GB</td>
<td>44.1</td>
<td>49.0</td>
</tr>
<tr>
<td>MyDigitalSSD MDSSD32MLC-S 32GB MLC</td>
<td>31.6</td>
<td>113.0</td>
</tr>
<tr>
<td>MTRON_MSD-SATA3025 16GB</td>
<td>65.4</td>
<td>74.6</td>
</tr>
<tr>
<td>RiDATA NSSD-S25-16-C02T 16GB</td>
<td>49.5</td>
<td>54.5</td>
</tr>
<tr>
<td>MEMORIGHT MR25.1-016s</td>
<td>81.5</td>
<td>97.1</td>
</tr>
</tbody>
</table>
Performance Test

- Windows Boot Time

<table>
<thead>
<tr>
<th>Product</th>
<th>Boot Time (Seconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SanDisk SDS5C-032G-102500 A-3.13</td>
<td>0.46</td>
</tr>
<tr>
<td>SAMSUNG_MCBQE64GBMP-03A 64GB</td>
<td>0.44</td>
</tr>
<tr>
<td>MyDigitalSSD MDSSD032MLC-S 32GB MLC</td>
<td>1:36</td>
</tr>
<tr>
<td>MTRON_MSD-SATA3025 16GB</td>
<td>0.43</td>
</tr>
<tr>
<td>RIDATA NSSD-S25-16-C02T 16GB</td>
<td>0.47</td>
</tr>
<tr>
<td>MEMORIGHT MR25.1-016s</td>
<td>0.45</td>
</tr>
</tbody>
</table>
Performance Test

• **Windows 7 SSD Performance Requirement**
  - Please report SSD ad non-rotation media base on ATA8- ACS1
  - Disk Sequential 64K Byte Read > 25 MB/s
  - Disk Random 16K Byte Read > 0.5MB/s
  - Disk Sequential 64K Byte Write > 20 MB/s
  - Average Read Time with Sequential Writes < 25 ms
  - Latency: 95th Percentile < 120 ms
  - Latency: Maximum < 700 ms
  - Average Read Time with Random Writes < 40 ms
OS Independent Test

Mechanical Test

- Mechanical Test
  - For Signal and Power Connector: (SATA CabCon MOI for Calipers, Page 30~33, Page 35~37)

Example: From the centerline of the side mounting holes to the top of the tongue of the SATA plug should be 0.50 ± 0.38 mm.
Electrical test

- SATA OOB Test (PHY out of Band)

<table>
<thead>
<tr>
<th>Model Name</th>
<th>Type</th>
<th>Manufacture</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDS6154C</td>
<td>Digital Storage Oscilloscope</td>
<td>Tektronix</td>
<td>15GHz Band Width / 40Gs Sample rate</td>
</tr>
<tr>
<td>AWG 7102</td>
<td>Arbitrary Waveform Generator</td>
<td>Tektronix</td>
<td>10GHz</td>
</tr>
</tbody>
</table>
Reliability Test

- Disk Stress for 7 days
  - Allion Disk Stress Utility
  - More than 3GB test Data Files (Large size files and Large number small size files)
  - File transfer and data compare
  - Without any system error and data lost
  - Failure rate about 70%
OS Independent Test

Reliability Test
• Temperature Extreme Test

Equipment
- Temperature Range: -40 °C to +100 °C (±0.2°C)
- Humidity Range: 0% ~ 98%RH (±2.5%RH)
- Temperature Change Speed:
  - 25 °C to 100 °C: 30 Minutes
  - 25 °C to -40 °C: 50 Minutes
- Test Space Size: 50cm (W) x 75cm (H) x 60cm (D)
- Material: SUS304 Stainless Steel
Reliability Test

• Endurance Test
  ṭ Depend on the method in JEDEC 64.8 that recommend from Intel
  ṭ Long term Endurance with vendor define workload
Retention Test

- Depend on the method in JESD47F from JEDEC
  - The extrapolated mean Data retention lifetime at 25°C is about 3 year while operating the DUT under 75°C over 96 hrs

- Long term Data Retention
  - Follow the Customer request or Allion suggestion to setting the Temperature and Humidity
OS Independent Test

Reliability Test

- Power Cycling Test
  
  Power Off/On the SSD then make sure the SSD can report correctly data in 1.5 seconds. (Repeat the testing for 1000 times)

Tool: DriverMaster Version

  DriverMaster Power Supply
Thank You

Coming Up:
Q&A
Q & A

1. SATA Compliance Test Introduction
2. SATA Certified Logo V1.3 Update
3. SATA UTD V1.4 Information
4. SATA Certified Logo Process
5. SATA SSD Testing

Thank you for your attention! J