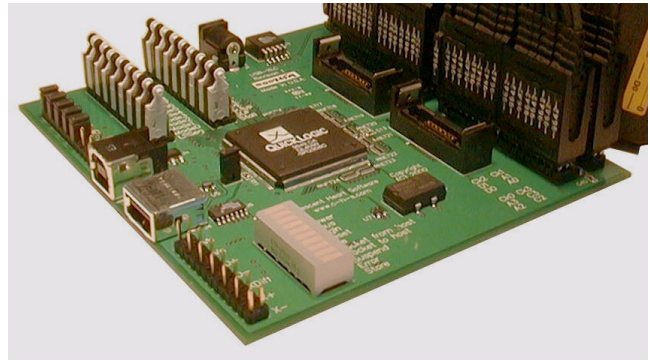
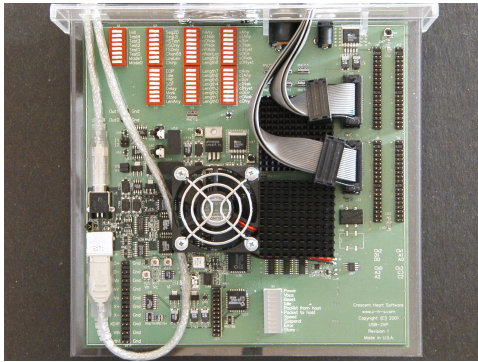


INDUSTRIAL-STRENGTH USB PROBING PRODUCTS

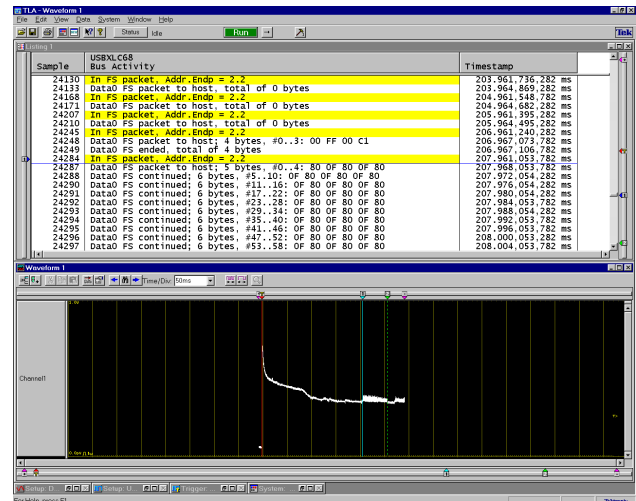
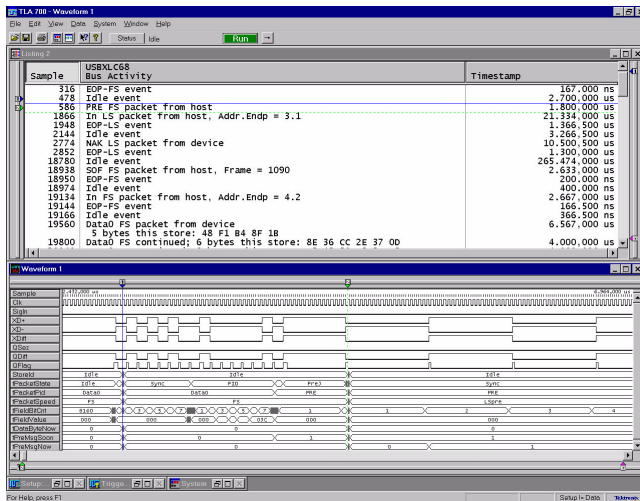
For Use With Tektronix® Logic Analyzers



USB-2XP shown with case open and high-density probes (left) and USB-XLC with standard logic analyzer probes (right)

USB-2XP: High performance probing of USB2.0/1.1/1.0 systems

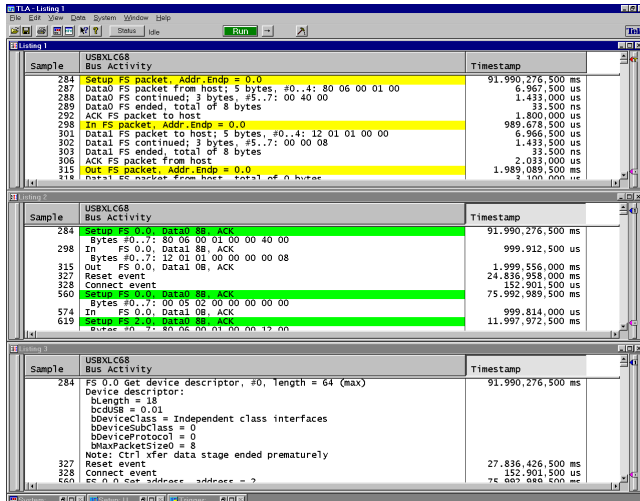
- Highest-performance USB2.0/1.1/1.0 probing available, with three cost-performance models
- Probes high-speed (HS), full-speed (FS) and low-speed (LS) bus traffic, including USB OTG sequences
- Proprietary high-performance front-end circuitry with non-repeater probing connection
- Minimal high-speed signal distortion achieved via ultra-short USB signal path (0.35" (8,9 mm))
- Acquires and displays low-level HS/FS/LS bus signaling, with bit-, field- and packet-level annotation
- High-speed signaling timing resolution of 694 ps (1.44 GHz (3x oversampling) rate)
- Acquires and displays all facets of USB behavior, including: low-level signaling; chirp speed negotiation; suspend, resume, other bus events; packets; transactions; control transfers with device class decoding
- Seamless tracking of bus activity across USB2.0 and USB1.1/1.0 domains
- Ten LEDs provide visual indication of Vbus, Reset, Idle, Packet-from-host, Packet-to-host, Speed, Suspend, Error and other activities (continuously functional)
- Continuously tracks bus utilization, error statistics on address or endpoint basis, continually reportable
- Works with Tektronix® TLA5xxx/6xx/7xx logic analyzers with 34-channel minimum (68-channel recommended) 100 MHz acquisition modules, high-density (recommended) or standard probes, compression probes supported with use of "Mictor-on-the-PCB" adapters
- Highly efficient use of acquisition memory: two samples used for most bus events and packets, with data packets averaging three bytes per sample (for 34-channel acquisition; 2x improvement for 68 channels)
- Supports simultaneous connection of multiple acquisition modules
- Jumper-controlled Vbus disconnection facilitates re-enumeration without unplugging cables
- Dip switch controlled selections optionally suppress acquisition of PRE and/or SOF bus packets
- Dip switch controlled selections optionally suppress acquisition of Chirp, EOP and/or Idle bus events
- Dip switch controlled selections optionally suppress acquisition of data bytes, 2-1024 bytes specifiable
- Dip switch controlled selections optionally mark and/or suppress acquisition of any or all of 22 different types of transactions (including In-NAK, Out-NAK, Ping-NAK and Ping-ACK)
- Decoding of packet activity into byte-wide streaming data to further facilitate triggering
- Packet and event duration tracking performed by hardware, independent of logic analyzer timestamping
- Probe adapter detects 7 packet errors and 24 event errors, which can be triggered on
- Test point access to monitor buffered versions of D+ and D- signals and USB xcvr X+, X- and XDiff outputs
- Test point access to monitor Vbus voltage and current (as 0.1 Ohm sensing-resistor voltage drop)
- Test point access to monitor Vbus current, as output of wideband current-to-voltage amplifier with jumper-selectable gain of X1 to X100, permitting measurements of Vbus inrush current, connect current, operating current and suspend current when using a digital multimeter or DSO
- Test point access to monitor occurrence of SOF packets
- Test point access to monitor high-speed D+/D- differential analog waveform, disconnect signal output
- Test point access to monitor normal-, chirp- and disconnect-level HS thresholds, thresholds are adjustable



Left: Listing window event- and packet-level display of full- and low-speed bus traffic, along with time-coordinated low-level bus activity waveform display. **Right:** Similar listing display (with start-of-transaction packets highlighted) of USB video camera packet activity, along with time-coordinated DSO waveform display of Vbus current used by the camera as monitored by USB-2XP. DSO vertical scale is 1A; the Vbus current spikes to 0.75A when the camera is turned on (at "T"), with variations in current seen when isochronous transfers begin (from "1" (seen in listing too) to "2").

USB-XLC: Extremely low cost probing for USB1.1/1.0 systems

- Highest performance USB1.1/1.0 probing available
- Probes full-speed (FS) and low-speed (LS) bus traffic
- Acquires and displays low-level FS/LS bus signaling, with bit-, field- and packet-level annotation
- FS/LS signaling timing resolution of 16.7 ns (60 MHz (5x FS oversampling) rate)
- Acquires and displays all facets of USB behavior, including: low-level signaling; suspend, resume and other bus events; packets; transactions; control transfers with device class decoding
- Ten LEDs provide visual indication of Vbus, Reset, Idle, Packet from host, Packet to host, Suspend, Error and other activities (continuously functional)
- Works with Tektronix® TLA5xx/6xx/7xx logic analyzers with 34- or 68-channel 100 MHz (standard) acquisition modules (68 channels recommended), high-density (recommended) or standard probes, compression probes supported with use of "Mictor-on-the-PCB" adapters
- Highly efficient use of acquisition memory: two samples are used for most bus events and packets, with data packets averaging three bytes per sample (applies for 34-channel acquisition; 2X improvement for 68-channel acquisition)
- Supports simultaneous connection of multiple acquisition modules
- Jumper selection to optionally suppress acquisition of any or all types of bus packets (ACK, Data0, Data1, In, NAK, Out, PRE, Setup, SOF, Stall)
- Jumper selection to optionally suppress acquisition of any or all types of bus events (Connect, EOP, Idle, Reset, Resume, Suspend)
- Jumper-controlled selections optionally suppress acquisition of data bytes, with acquisition of up to the first 2-1023 bytes specifiable
- Probe adapter provides packet and event duration tracking, independent of logic analyzer timestamping
- Probe adapter detects 13 packet errors and 4 event errors, which can be triggered on
- Test point access to monitor USB D+ and D- bus signals and transceiver X+, X- and XDiff outputs
- Test point access to monitor Vbus voltage
- Test point access to monitor Vbus current, as voltage drop across a series 0.1 Ohm sensing resistor, permitting measurements of operating and suspend currents when using a digital multimeter; use of a DSO with a differential probe additionally allows measurements of inrush and connect currents to be made
- Test point access to monitor occurrence of SOF packets
- Probe adapter provides test modes to verify functioning of probe adapter and proper probe connection to logic analyzer



Left: Acquisition of USB device enumeration bus activity shown in three related listing display windows: basic-level bus event and packet display (with start-of-transaction packets highlighted, and display of EOP and Idle events as well as SOF packets suppressed) (top); transaction-level display (with setup transactions highlighted) (middle); control transfer-level display (bottom). Right: Multi-window display of DSO capture of full-speed D+ and D- signals (top), along with low-level logical view of the same signaling (middle), plus high-level event/packet protocol interpretation (bottom).

Software Features

- Graphical user interface support for complex multi-state logic analyzer trigger programs
- Powerful debug capabilities for triggering on and/or selective storage of events, packets and transactions
- Trigger on and/or selective acquisition of real-time bus anomalies as well as normal bus behavior
- Optionally trigger on packet byte-wide streaming data (USB-2XP)
- System software inherently supports time-coordinated display of multiple listing and waveform windows, along with window-linked cursor control
- System software has multiple display modes for analyzer-acquired timestamp information with 500 ps timing resolution (time from prior-displayed event, from system trigger occurrence, or absolute time)
- Listing window high-level hierarchical display shows bus events and packets, transactions or control transfers, the latter with device class decoding
- Low-level waveform display of bus activity can be viewed via a waveform window (for full- and low-speed traffic) or in a listing window (for high-speed traffic)
- Logic analyzer system software provides facilities to search listing and waveform windows for text or data information of interest
- Continually-updated histogram display of continuously-acquired bus utilization statistics (USB-2XP/C)
- Listing display controls affecting error, radix, control transfer details, event/packet duration, packet speed, packet direction and packet locality displays are provided
- Address-endpoint-based selective display controls provided (address-endpoint, mask, direction)
- Split-transaction-related selective display controls provided (hub address, hub address mask, hub port, hubport mask, endpoint type)
- Controls provided to enable/disable display of transactions based on the packet types present or absent in the transaction
- Controls allow suppression of display of trailing data bytes of lengthy data packets, complementing the hardware-implemented selective storage facility which can suppress the storage of such data bytes
- Controls provided to suppress display of specified types of acquired bus events
- System software supports multiple acquisition modules, allowing time-coordinated probing and display of USB activity along with e.g. that of the USB device- or USB host-processor, with high-level source code language display supported
- USB-2XP: 6 acquisition controls with 15 total acquisition-related selections; 4 for USB-XLC
- USB-2XP: 82 display controls with 222 display-related selections; 52 controls, 146 selections for USB-XLC
- Well over 100 specific errors can be reported on
- Tektronix® TLAVu application allows off-line viewing on any Tektronix system, no logic analyzer required

Logic Analyzer System General Capabilities

- TLA5xxx systems are cost-reduction engineered to support a single logic analyzer acquisition module of 34-, 68-, 102- or 136-channels, with 235 MHz state acquisition rates, 800 MHz asynchronous acquisition rate
- TLA7xx systems support multiple logic analyzer acquisition, digital oscilloscope (DSO) as well as digital pattern generator modules; TLA7Axx systems have increased throughput
- Acquisition modules provide 2 Ghz MagniVu timing acquisition and display for general-purpose debug
- Acquisition timestamping with 500 ps resolution
- Windows system with familiar user interface, as well as floppy-disk and CD-ROM drives, built-in LAN networking and USB ports
- Multiple, time-coordinated listing and waveform display windows
- Graphical trigger program facility with up to sixteen highly complex trigger states and multiple 51-bit counter/timers
- Tektronix TLAVu application runs on any desktop or laptop Windows system, allowing off-line viewing

USB Probing Products Ordering Summary

USB-2XP

- Includes USB-2XP probe adapter, power supply, AC power cord and software
- Model USB-2XP/A probes HS/FS/LS traffic using 34-channel acquisition
- Model USB-2XP/B additionally supports 68-channel acquisition, use of which provides for: 2x more efficient use of acquisition memory; facilitation of complex trigger constructs; optional acquisition and annotated display of low-level FS/LS bus behavior (sampled at 60 MHz)
- Model USB-2XP/C additionally provides support when using 68 channel acquisition for: optional acquisition and annotated display of low-level HS bus behavior (sampled at 1.44 GHz); continuous tracking and optional continual reporting of bus utilization and error statistics
- USB-2XP/A, /B and /C separately-orderable components:
 - USB-2XP/A-HW (hardware)
 - USB-2XP/A-SW (software, includes 34- and 68-channel versions)
 - USB-2XP/B-UP (upgrade from model A to model B, in-the-field upgradable)
 - USB-2XP/C-UP (upgrade from model B to model C, in-the-field upgradable)
- USB-2XP pricing provided upon request

USB-XLC

- Includes USB-XLC probe adapter, power supply, AC power cord and software
- Probes FS/LS traffic using 34- or 68-channel acquisition modules; provides for acquisition and annotated display of 60 MHz-sampled FS/LS bus behavior when using 68 channel acquisition modules
- USB-XLC separately-orderable components:
 - USB-XLC-HW (hardware)
 - USB-XLC-SW (software, includes 34- and 68-channel versions)
- USB-XLC pricing provided upon request

Contact Crescent Heart Software

- Internet: www.c-h-s.com; E-mail: sales@c-h-s.com; Voice: (+1)503-232-2232; Facsimile: (+1)503-232-2255
- Crescent Heart Software, a Tektronix® Embedded Systems Tools Partner and a member of the Tektronix® Logic Analyzer Third Party Developer team, is headquartered in Portland, Oregon USA.
- Crescent Heart Software has been a member of the USB Implementer's Forum (USB-IF), and has provided technical consultation and feedback regarding electrical signaling issues to the Version 1.1 and 2.0 USB specification definers.
- Note that this datasheet (best viewed directly from Acrobat; select Print As Image to print), sample acquisition files and probing software are available for download from our website. Note that a logic analyzer is not required to run the software; please contact CHS technical support for details.
- Information presented herein is subject to change without notice (datasheet Rev. P, September 2004)